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International Conference on Compliant & Alternative Substrate Technology

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ICAST Program

Sunday, 19 September 1999 - Welcoming Reception - 7:30 p.m. - 9:00 p.m. - Marvin Gardens

	Speaker Name/Topic
Session 1: Monday AM 20 September (8:40 am - Noon) - SUBSTRATE CREATION	
CHAIR: TERESA MAYER	**ROOM: MARVIN GARDENS A & B**
7:45 a.m. - 8:40 a.m. - Registration & Continental Breakfast	
8:40 a.m. - Welcome & Orientation - Matt Seaford	
9:00 a.m. - 9:30 a.m. (Scene-setter)	Yu-Hwa Lo - Recent Progress in Compliant Substrates
9:30 a.m. - 9:50 a.m.	Qin-Yi Tong - Transfer of Semiconductor and Oxide Films by Wafer Bonding and Layer Splitting
9:50 a.m. - 10:10 a.m.	Igor Malik - Compliant SOI Substrates
10:10 a.m. - 10:30 a.m.	Peter Moran - Strain Relaxation in Bonded Compliant Substrate Structures
Break: 10:30 a.m. - 10:40 a.m.	
10:40 a.m. - 11:00 a.m.	Theresa Mayer - Use of Wafer Bonding for Enhancements in Device Performance
11:00 a.m. - 11:20 a.m.	William Jesser - Selection of Compliant Substrates
11:20 a.m. - 11:40 a.m.	James Speck - Approaches to Low Threading Dislocation Density Materials and Related Modeling
11:40 a.m. - 1:00 p.m. - **Lunch**	**ROOM: MARVIN GARDENS C**
Session 2: Monday PM (1:00 pm - 4:00 pm) - WAFER BONDING STUDIES	
CHAIR: PETER MORAN	**ROOM: MARVIN GARDENS A & B**
1:00 p.m. - 1:30 p.m. (Scene-setter)	Ulrich Goesele - Compliant Substrates by Twist Wafer Bonding: Fact or Fiction?
1:30 p.m. - 1:50 p.m.	Stefan Bengtsson - Low Temperature Wafer Bonding
1:50 p.m. - 2:10 p.m.	Cindy Colinge - Processing of Silicon for Three-Dimensional Applications
2:10 p.m. - 2:30 p.m.	Russell Dupuis - Wafer Bonding for InP Materials and Devices
Break: 2:30 p.m. - 2:50 p.m.	
2:50 p.m. - 3:10 p.m.	Matt Seaford - Comparison of InGaSb/InAs Superlattice Structures Grown by MBE on GaSb, GaAs, and Compliant GaAs Substrates
3:10 p.m. - 3:30 p.m.	Kent Choquette - Compliant Substrates and Optoelectronic Device Integration by Wafer Bonding
3:30 p.m. - 3:50 p.m.	Mark Sheplak - Aerodynamic Sensors Using Silicon Nitride Wafer-Bonding Technology
Session 3: Tuesday AM 21 September (8:40 am - 12:00 noon) - DETECTORS	
CHAIR: MATT SEAFORD	**ROOM: MARVIN GARDENS A & B**
8:00 a.m. - 8:30 a.m. - Continental Breakfast	
8:30 a.m. - 9:00 a.m. (Scene-setter)	C.H. Thompson Lin - Study of InGaAs/GaAs Compliant Substrates for Various Applications
9:00 a.m. - 9:20 a.m.	John Roth -Alternative Approach to the Growth of HgCdTe IR Detectors
9:20 a.m. - 9:40 a.m.	Koen Vanhollebeke - InGaAs Layers Grown by OMVPE on Compliant Substrates for Extended Wavelength Detectors
9:40 a.m. - 10:00 a.m.	Gail Brown - Strained-layer InAs/InGaSb Superlattices on Compliant GaAs Substrates for Very Long Wavelength Infrared Detection
Break 10:00 a.m. - 10:20 a.m.	
10:20 a.m. - 10:40 a.m.	Wen Wang - GaAs Growth on SOI (Presented by Matt Seaford)
10:40 a.m. - 11:00 a.m.	Louis Kilmer - Compliant and Alternative Substrate Requirements for Low Cost, Light Weight, High Efficiency Solar Cells
11:00 a.m. - 11:20 a.m.	Richard King - Compliant Substrates for Multijunction Photovoltaic Cells

	Speaker Name/Topic
Session 3: Tuesday AM 21 September (8:30 am - 12:00 noon) - DETECTORS, CONTINUED	
11:20 a.m. - 11:40 a.m.	Andrew Allerman - Potential Applications of Compliant Substrates in Opto-electronics and Photovoltaics
11:40 a.m. - 12:00 noon	Robert Davis - Lateral and Pendeo-epitaxial Growth of GaN and Related Compounds and Alloys on 6H-SiC(0001) and Si(111) Substrates
12:00 noon - 1:00 p.m. - **Lunch**	**ROOM: MARVIN GARDENS C**
NOTE: Tuesday afternoon free; Tuesday night = Reception and Banquet 7:00 p.m. - 9:30 p.m. **ROOM: SEABREEZE POINT (OUTDOORS - WEATHER PERMITTING) OR MARVIN GARDENS**	
Session 4: Wednesday AM 22 September (8:40 am - 12:00 noon) - WIDE BANDGAP MATERIALS **CHAIR: APRIL BROWN**	**ROOM: MARVIN GARDENS A & B**
8:00 a.m. - 8:40 a.m. Continental Breakfast	
8:40 a.m. - 9:10 a.m. (Scene-setter)	Dimitris Pavlidas - GaN on Silicon-on-Insulator (SOI) Substrates and Compliant Growth of Wide Bandgap Materials
9:10 a.m. - 9:30 a.m.	April Brown - Compliant Substrates for GaN and Strain Modulated Epitaxy
9:30 a.m. - 9:50 a.m.	Ling Zhang - Lateral Epitaxial Overgrowth Using Alternative Sources
9:50 a.m. - 10:10 a.m.	David Zubia - Nanostructured SOI Compliant Substrates
Break: 10:10 a.m. - 10:20 a.m.	
10:20 a.m. - 10:40 a.m.	Mike Mazzola - Chemical Vapor Deposition of 3C-SiC on Silicon Compliant Substrates
10:40 a.m. - 11:00 a.m.	Mike Spencer - Growth of SiC and III-V on Polycrystalline SiC Substrates Utilizing Wafer Bonded Single Crystal Si Template
11:00 a.m. - 11:20 a.m.	Nader Kalkhoran - Systematic Study of SIMOX SOI Structures as Compliant Substrates for SiC and GaN
11:20 a.m. - 11:40 a.m.	Richard Woodin - Compliant Substrates for Silicon Carbide Growth
11:40 a.m. - 1:00 p.m - **Lunch** followed by afternoon free	**ROOM: MARVIN GARDENS C**
Session 5: Wednesday PM (6:30 pm - 9:30 p.m.) - ELECTRONIC AND OPTO-ELECTRONIC DEVICES **CHAIR: STEVEN PEI**	**ROOM: MARVIN GARDENS A & B**
6:30 p.m. - 7:00 p.m. (Scene-setter)	Fred Kish - Recent Advances in High-Brightness Transparent-Substrate AlGaInP Light-Emitting Diodes: The Road Towards Viable Solid-State Lighting Sources
7:00 p.m. - 7:20 p.m.	Felix Ejeckam - Title TBA
7:20 p.m. - 7:40 p.m.	Karl Hobart - Compliant Substrates: A Comparative Study of the Relaxation Mechanisms of Strained Films Bonded to High and Low Viscosity Oxides
7:40 a.m. - 8:00 p.m.	Steven Pei - Compliant Substrate for High Power Optically Pumped Mid-IR Lasers Applications
Break: 8:00 p.m. - 8:10 p.m.	
8:10 p.m. - 8:30 p.m.	Prashant Chavarkar - Strain Relaxation in $In_xGa_{1-x}As$ Lattice Engineered Substrates
8:30 p.m. - 8:50 p.m.	Patricia Mooney - SiGe FET Structures on Silicon-on-Sapphire Substrates
8:50 p.m. - 9:10 p.m.	Glenn Martin - Boeing Interests
9:10 p.m. - 9:30 p.m.	John Jensen - HRL Interests
Wrap-up Session: Thursday AM - 23 September - (8:00 am - 11:00 am) **ROOM: MARVIN GARDENS A & B**	

Transfer of Semiconductor and Oxide Films by Wafer Bonding and Layer Splitting

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Material integration by wafer bonding and layer transfer is one of the main approaches to increase functionality on Si and to improve integrated circuits (IC) performance. The key to a successful wafer bonding is sufficiently high attraction forces at the bonding interface. The bonding surfaces must be sufficiently smooth so that the intermolecular forces between them is large enough to elastically deform the not-perfectly-flat surfaces to conform each other. In order to prevent interface thermal bubbles and to provide high bonding forces, the bonding surface must also be terminated only by few designed monolayers of bonding species or fresh atoms of themselves. If above conditions can be met, bonding of any wafers appears to be feasible. The use of a bonding having a well-developed surface preparation technology layer on hard-to-prepare wafer surfaces is an alternative way to realize bonding.

Even though most mismatches between bonding materials present no obstacle for wafer direct bonding, thermal stresses caused by thermal mismatches must be minimized by low temperature bonding. To achieve a strong bond at low temperatures, two approaches can be adopted: 1) bonding at room temperature by hydrogen bonding of OH, NH or FH terminated surfaces followed by polymerization to form covalent bonds. The key is to remove the by-products of the reaction at the bonding interface and 2) direct formation of a covalent bond between fresh and high energy atoms in UHV or in ambient. Low temperature bonding allows bonding operation at wafer level for manufacturing.

Layer transfer requires uniform thinning of one wafer of a bonded pair. The most promising technology for that is to emblettle the region underneath the wafer surface corresponding to the layer thickness by H or other ion implantation. The layer is then transferred onto a bonded desired substrate by splitting due to internal gas pressure or by forced peeling as long as the bonding energy is higher than the fracture energy in the emblettled region at the layer transfer temperature. This approach is quite generic in nature and may be applied to almost all materials. We have found that B+H co-implantation and/or H implantation at high temperatures can significantly lower the splitting temperature. However, the wafer temperature during H implantation has to be within a temperature window that is specific for each material. The experimentally determined temperature windows for some semiconductors and single crystalline oxides will be given.

Compliant SOI Substrates: Preliminary Research Data

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Silicon Genesis Corporation, Campbell, CA

and AnnaLena Thilderkvist
Applied Materials, Santa Clara, CA

Compliant substrates are used for growing thin heteroepitaxial films for a variety of electronic applications. The key obstacle to overcome is to manage the lattice mismatch between the thin film and the substrate. Typically, the lattice mismatch results in a high level of strain that relaxes through formation of dislocations; the density of these dislocations is often too high for the resulting material to be useful for electronic devices.

One strategy for the generation of compliant substrates – substrates that can effectively deal with the lattice-mismatch-related strain – is to prepare an ultrathin SOI (Silicon-on-Insulator) wafer in which the underlying BOX (buried oxide) accommodates the overlayer strain without the creation of dislocations [1, 2]. The main challenge in this strategy is to maintain a reasonable thickness uniformity of the SOI overlayer that is typically only ~<200 A thick to be effective as a compliant substrate.

We discuss a modified process flow for SOI substrate manufacturing that uses a new approach to SOI layer surface finishing. While CMP (chemical-mechanical polishing) is usually applied to reduce the SOI surface roughness, we show that by using Si epi technology one can achieve SOI uniformity and surface roughness levels in line with the compliant substrate requirements.

8" diameter wafers were used in this preliminary study for research and development purposes only. The surface finishing using the epi technology resulted in <200 A average SOI thickness with ~50% range. The feasibility of ~100 A thick SOI layers with surface roughness ~1 A rms (2x2 micron AFM) was demonstrated as well. It is reasonable to expect further improvements of the film uniformities through further process optimization.

References:

[1] Z. Yang, J. Alperin, W. I. Wang, S. S. Iyer, T. S. Kuan, and F. Semendy, JVST B 16 (3), 1489-1491 (1998).

[2] U. S. Patent 5,759,898.

Strain Relaxation in Bonded Compliant Substrate Structures

P.D. Moran*, D.M. Hansen*, L.J. Mawst, J.G. Cederberg*, B. Hawkins*, T.F. Kuech*
* Department of Chemical Engineering, ** Department of Electrical Engineering
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Many techniques can be used to form the thin template layers (<10nm) comprising the critical layer in a compliant substrate. While many approaches can lead to the same final physical structure to the compliant substrate, the details of the substrate formation process can lead to variations in the film quality of materials grown on the compliant substrate. We investigated two different bonding structures that nominally yield the same final compliant substrate structure. In both cases, borosilicate glass (BSG) is used as a bonding and compliant medium, however the placement of the bonding interface is different. One type of substrate consists a CVD-deposited BSG layer on a GaAs handle wafer-bonded directly to the GaAs template layer (glass-to-GaAs samples). The formation of this substrate requires both the application of high pressures (1-10 MPa) and moderate temperature (550°C) during the bonding process. The second substrate consists of CVD-deposited BSG on both the GaAs template layer and the handle wafer. In this case, the wafer bond is formed between the two BSG surface at room temperature and no externally applied pressure (glass-to-glass substrates). These latter substrates have BSG glass directly deposited on the GaAs surface. All the substrates were chemically thinned to the template layer and prepared through a series of etches just prior to introduction into the MOVPE system and subsequent growth.

The glass-to-GaAs bonded samples were used in the study of the growth of high and low latticed mismatched $In_xGa_{1-x}As$. $In_{0.45}Ga_{0.55}As$ layers were grown to a thickness of 2 μm, well beyond the conventional critical thickness. X-ray diffractometry was used to determine the effect of the bonding interface on the resulting strain relaxation in the growing films. The use of the glass-to-GaAs bond reduced the breadth of the strain distribution and resulted in a significantly smoother surface as seen by AFM than that obtained by growth on a conventional substrate. $In_{0.03}Ga_{0.97}As$ and $In_{0.09}Ga_{0.91}As$ layers were also grown on these substrates to a thickness of ~0.1 μm, on the order of the conventional critical thickness. In this case, the films grown on the bonded substrates were pseudomorphically strained to the same degree as the films grown on the conventional substrate. Within this type of bonded structure, the relaxation of subsequently grown films only occurs in the presence of dislocations (or other defects) that result from growth well beyond the conventional critical thickness.

$In_{0.45}Ga_{0.55}As$ layers grown on the substrates with the glass-to-glass bond to a thickness of 2 μm do not exhibit the same reduction in surface roughness as those films grown on the substrates with the glass-to-GaAs bond. This result suggests that type and position of the bonded interface, or the direct deposition of the CVD-BSG layer, affects mechanism of the strain relaxation of mismatched films grown beyond their critical thickness.

Use of Wafer Bonding for Enhancements in Device Performance

James Matzella, Dmitri Lubyshev, Paul Roman, Jerzy Ruzyllo, David Miller, and Theresa Mayer
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Materials integration using wafer bonding has gained attention recently due to enhancements that can be obtained in the performance of many optical and electrical devices, including high-brightness LEDs, low-power CMOS devices, and silicon power devices. Moreover, the use of wafer bonding to form compliant substrates is being considered to address the growth of lattice-mismatched materials, thereby allowing introduction of devices fabricated from emerging semiconductor materials including the antimonides and the III-nitrides. At this workshop, we will discuss research that is being performed at Penn State University to address the use of dry (gas phase) surface chemistries as a final conditioning step prior to hydrophobic silicon wafer bonding for silicon power devices. The surface conditioning process and bonding procedure will be described and a comparison of surface energy measurements on wet and dry processed wafers will be presented. We will also provide an overview of activities that are underway to develop a GaAs-based compliant substrate technology and results that have been obtained on the growth of lattice-mismatched $In_xGa_{1-x}As$ on these substrates. The first approach that will be discussed uses lateral wet AlAs oxidation to form an oxide layer that separates the GaAs compliant layer from the host substrate. The second technique utlizes a "plastic" interlayer of Sb-based materials that softens at the growth temperature of the lattice-mismatched layers.

SELECTION OF COMPLIANT SUBSTRATES

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Experimental results show that significant improvements in the crystalline perfection of heteroepitaxial films, HEF, can be achieved by twist-bonding an intermediate layer of substrate material to a bulk substrate, BS. The hope is for this intermediate layer to act as a compliant substrate, CS, so that any film may be epitaxially grown on it with a high degree of perfection. In this paper an elastic misfit accommodation model is developed to address several issues. Is there is a limit to the amount of misfit that can be accommodated by the compliant substrate? What is the role of the array of interfacial screw dislocations? What design criteria are suggested by the model? The following broad guidelines result from the model.

- The role of the screw dislocation array is to provide pre-existing dislocations that can reorient to accommodate misfit between the elastically distorted compliant substrate and the bulk substrate.
- A large angle of twist produces a large density of screw dislocations, which facilitates elastic distortion of the CS by reducing the energy barrier to reorientation of the dislocations. An estimate of the minimum effective twist-angle is roughly 8 degrees, and coincidence angles should be avoided.
- According to the model, it is difficult to expect misfit more than about 10% to be accommodated elastically by the CS. Above this misfit the HEF is expected to generate misfit dislocations at the HEF/CS interface.
- The CS should be of a softer elastic constant relative to the HEF and have as small a thickness as is practical. If the thickness is too small the array of screw dislocations can be lost to the free surface and hence their benefit is also lost.
- The CS should be chosen to have a large misfit with the BS and a small misfit with the HEF. Twist bonding a material of lattice constant near that of the HEF is better than twist bonding a layer of lattice parameter equal to that of the BS.
- The CS should be of a material that the HEF can grow in a 2-D, layer-by-layer growth mode so that the dislocations and planar defects introduced during island coalescence are avoided.

In the quantitative development of the model for elastic accommodation of misfit the basis for the above selection criteria are given. The model is based on accommodation of misfit by elastic deformation of the CS and the HEF. In cases where the HEF and the CS plastically deform to accommodate the misfit by introducing misfit dislocations other considerations than those above become significant. In this case of plastic deformation the criteria for selection of a compliant substrate can be made on the basis of attracting the misfit dislocation segments threading through the HEF into the HEF/CS interface or into the CS/BS interface. Such a process requires time for the dislocations to move under local stresses that exceed a frictional stress.

Approaches to Low Threading Dislocation Density Materials and Related Modeling

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In this presentation, we consider novel approaches to achieving low threading dislocation density materials. The compliant approach requires a thin substrate (compliant layer (CL)) which must be able to *slide* over a host substrate in order to either elastically or plastically deform to the lattice parameter of a subsequently grown misfitting layer. To date, there has not been any experimental data that has clearly demonstrated mesoscopic interfacial sliding during the growth of misfitting layers on CLs. Here, we consider experimental approaches in which a misfitting layer relaxes through plastic processes involving threading dislocation (TD) and misfit dislocation (MD) generation. In normal misfitting layer growth on thick substrates, TD motion is limited by blocking by the elastic field of MDs which lie on intersecting slip planes - this blocking in the usual case leads to further TD generation and subsequent high TD densities. When TD blocking can be avoided or minimized, it should be possible to grow low defect density layers. Here we show that this is a common theme for graded layer growth, lattice engineered substrates (via lateral oxidation), and growth on thin layers fused on low viscosity glasses.

Compliant Substrates by Twist Wafer Bonding: Fact or Fiction?

U. Gösele, St. Senz, R. Scholz, T. Akatsu, A. Plößl, P. Kopperschmidt, and G. Kästner
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Reports by the group of Lo and co-workers at Cornell University that 'universal compliant substrates' may be fabricated by transferring a few nanometer thick layers of GaAs onto a GaAs substrates by twist wafer bonding have generated interest and research activities all around the world. From a theoretical point of view it turned out that the resulting 'grain boundary' will not allow sufficient movement over macroscopic distances required for compliancy. Alternatively, it had been suggested that correlated movement and annihilation of threading dislocations could locally relieve the misfit stress during the growth of a heteroepitaxial layer with a low remaining density of threading dislocations. Our experiments on the growth of InGaAs layers on twist bonded thin GaAs films on GaAs substrates indicate that the thin twist bonded GaAs layers either contain pin-holes causing grain boundaries where the threading dislocations are trapped or are relatively free of pin-holes and then contain bundles of threading dislocations. In both cases the behavior of the threading dislocations may be described by the conventional theory of misfit dislocation formation and does not require or indicate specific compliancy of the twist-bonded sandwich structure.

Although we could not realize 'universal compliant substrates' the associated experiments allowed us to perfect large area wafer bonding of III-V compounds at relatively low temperatures which is of interest for the fabrication of high efficiency LED's and VCSELs.

LOW TEMPERATURE WAFER BONDING

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Plasma assisted wafer bonding [1,2] has recently attracted attention as a low temperature bonding method. Very high surface energies have been reported after bonding at room temperature when using oxygen plasma exposure as preparation for wafer bonding. The mechanism of the plasma activation and the driving forces for the formation of covalent bonds at room temperature is still under debate.

In this work room temperature bonding properties were investigated when using O_2, Ar or N_2O plasmas as pre-bonding treatments. An STS Multiplex ICP Reactive Ion Etcher was used for the plasma activation of N-type silicon wafers. Different plasma exposure times were investigated and it was found that long exposure times degrade the bonding properties. A plasma exposure time of 30 s was chosen for most experiments. After plasma exposure some of the wafers were quickly dipped in DI-water and dried. The wafers were brought into contact at room temperature and left in clean-room ambient for about 24 h. The surface energy of the bonded interfaces was measured using the crack opening method. Results obtained after storage at room temperature for 24±3 h are summarized in Table I for O_2 and Ar plasmas. Results using conventional wet activation in SC1 is also shown for comparison. Surface energies corresponding to what can be achieved by activation in SC1 and annealing at 800°C have been obtained at room temperature.

Table I. Surface energies after storage of the bonded Si/Si pair 24±3 h at room temperature.

Surface activation	Surface energy (J/m^2) Plasma only	Surface energy (J/m^2) Plasma (or SC1) + DI-water
O_2 plasma	0.32	1.65
Ar plasma		0.85
SC1		0.102

Oxygen plasma was successfully used also for bonding of crystalline quartz to silicon and for bonding of thermal SiO_2.

Preliminary result using FTIR (Fourier Transform Infra-Red) spectroscopy shows very low traces of interfacial water after storage for 24 h at room temperature. Atomic Force Microscopy (AFM) investigations on plasma treated silicon surfaces reveal surface structures not found on silicon surfaces treated in SC1. From ellipsometric measurements the thickness of the oxide formed using 30 s of oxygen plasma was found to be roughly 50 _ (assuming n=1.46). Capacitance *vs.* voltage measurements on this oxide does not reveal any large charge content in the oxide. This result is in contrast to what has been reported by Farrens et al [2]. The interpretation of these results will be discussed.

Silicon/silicon structures bonded at room temperature using plasma activation has been electrically characterized to further reveal their properties and to investigate their usefulness for electronic applications.

1. S.N. Farrens, J.R. Dekker, J.K. Smith and B.E. Roberds, J. Electrochem. Soc. **142**, 3949 (1995)
2. S.N. Farrens, in Semiconductor Wafer Bonding IV, U. G^sele, H. Baumgart, T. Abe, C. Hunt and S. Iyer, Eds., **PV 97-36**, p. 425, Electrochem. Soc. Proc. Series, Pennington, NJ (1997)

Processing of Silicon for Three-Dimensional Applications

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Some of the recent challenges outlined in the 1997 Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) include: (1) reducing minimum feature size to increase the density of devices per chip, (2) maintaining constant drive current as power supply voltage is reduced, and (3) increasing the number of functions on a chip.

One approach that could double the density of devices per area without the need of new lithography would be to stack layers of devices in a three-dimensional structure. This idea is not new; device layers have been stacked by depositing polysilicon and using laser recrystallization to achieve a single crystal silicon layer. However, this approach was abandoned in the 1980's due to poor yield.

Low-temperature (T 450°C) silicon wafer bonding and hydrogen splitting is used here to transfer a thin layer of single crystal silicon to an intermediate handle wafer. The process allows access to front and backside of the transferred layer allowing the fabrication of double-sided devices capable of high current drive. Once transferred, a third device wafer is bonded to the thin-transferred layer followed by debonding of the intermediate wafer as shown in figure one. The intermediate bonding layer is a low-K dielectric polymer, which is applied by spin-on.

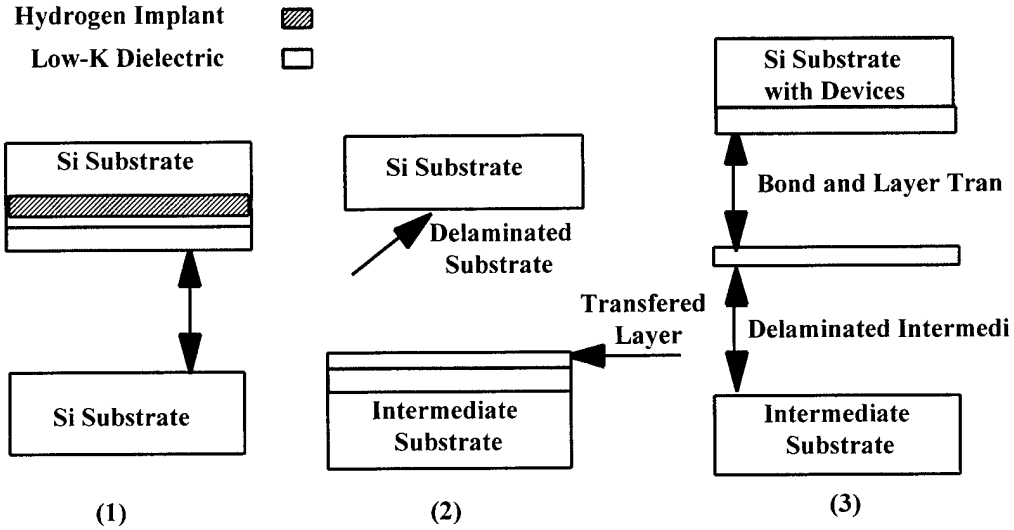

Figure 1: Schematic showing layer transfer of thin-film single crystal silicon.

Wafer bonding and hydrogen splitting have introduced a new technique for creating stacked single crystal device layers. In this presentation, recent research of layer stacking will be discussed.

Wafer Bonding for InP Materials and Devices

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Compliant substrate technologies have been investigated to overcome the limitation of epitaxial growth on lattice-matched substrates. For example, for the growth of In_xGa_xAs on InP substrates, the In alloy composition, x, should be $x \sim 53\%$ to achieve good quality epitaxial layers. In this work, the growth of strained InGaAs on InP-based compliant substrates using wafer twist bonding has been studied. Nomarski optical microscopy, atomic-force microscopy (AFM), and scanning electron microscopy (SEM) for examination of the surface morphology have been used to characterize the materials of this study. In addition, X-ray diffraction (XRD), transmission electron microscope (TEM), and photoluminescence (PL) have been employed to characterize the crystal quality of these heteroepitaxial layers. The results of the growth of various lattice-mismatched InGaAs heteroepitaxial films on InP-based compliant substrate and on standard InP substrate are described.

The InP "substrate" wafers to be twist-bonded are prepared using the following process. First, an InGaAs etch-stop layer and ~5 nm thick InP "compliant layer" are grown on a (100) InP substrate using low pressure metalorganic chemical vapor deposition (LP-MOCVD). Next, bonding is made at various relative orientations of the two InP crystallographic surfaces (e.g., 0, 10, 45 degrees), between the thin InP layer on the top of the as-grown wafer and a second (100) InP "host" substrate, which acts as a mechanically supporting substrate of the thin InP "compliant layer". Van der Waals bonding at room temperature is performed followed by direct fusion bonding at 600°C under various pressures. After bonding, the InP "host" substrate and the InGaAs "etch-stop" layer on thin compliant InP layer are removed. Finally, an intentionally lattice-mismatched InGaAs layer is grown on compliant substrate. Growth is also done on standard (100) InP substrate to compare with compliant substrate. As of this time, we have successfully grown InGaAs with a mismatch of up to 2% In (rich), resulting in a heteroepitaxial layer that is compressively strained.

Triple-axis XRD analysis of these films is used to create a reciprocal space map (RSM) for these layers in order to analyze the mosaic spread of lattice parameters in the InGaAs layers. Increased mosaic spread is related to increased dislocation density of the films. The RSM for the InGaAs/compliant substrate shows a smaller relaxed feature due to the strain accommodation of compliant substrate. Also, the XRD peak of mismatched InGaAs on the compliant substrate has a smaller mosaic spread than the "companion" InGaAs layer grown on standard substrate.

Comparison of InGaSb/InAs Superlattice Structures Grown by MBE on GaSb, GaAs, and Compliant GaAs Substrates

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This paper contains the characterization results for indium arsenide/indium gallium antimonide (InAs/InGaSb) superlattices (SL) that were grown by molecular beam epitaxy (MBE) on standard gallium arsenide (GaAs), standard GaSb, and compliant GaAs substrates. The atomic force microscopy (AFM) images, peak to valley (P-V) measurement, and surface roughness (RMS) measurements are reported for each sample. For the 5um x 5um images, the P-V heights and RMS measurements were 37 A and 17 A, 12 A and 2 A, and 10 A and 1.8 A for the standard GaAs, standard GaSb, and compliant GaAs respectively. The high resolution x-ray diffraction (HRXRD) analysis found different 0th order SL peak to GaSb peak spacings for the structures grown on the different substrates. These peak separations are consistent with different residual strain states within the SL structures. Depending on the constants used to determine the relative shift of the valance and conduction bands as a function of strain for the individual layers, the change in the InAs conduction band to InGaSb valance band spacing could range from +7meV to -47meV for a lattice constant of 6.1532A. The cutoff wavelength for the SL structure on the compliant GaAs, control GaSb, and control GaAs was 13.9mm, 11mm, and no significant response, respectively. This difference in cutoff wavelength corresponds to approximately a -23meV change in the optical gap of the SL on the compliant GaAs substrate compared to the same SL on the control GaSb substrate.

Compliant Substrates and Optoelectronic Device Integration by Wafer Bonding

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The requirement of near lattice-matching for conventional epitaxy techniques such as molecular beam epitaxy and metalorganic vapor phase epitaxy (MOVPE) impose a constraint on the intermixing of III-V and elemental semiconductors. Yet, there are numerous device technologies which would benefit through integration of materials with disparate lattice parameters, electronic properties, and/or optical properties. One technique to overcome epitaxial limitations is wafer bonding. This technique involves the atomic-scale fusion (covalent bonding) of the two different materials with a combination of pressure and high temperature. When successful, the resulting fused structure exhibits a disordered bonded interface with defects that are confined at the interface and thus have limited impact on the material properties away from the interface. Here we discuss the fabrication of compliant substrates and integration of optoelectronic devices using wafer bonding.

Wafer bonding extremely thin films (ò10 nm) twisted at an angle to carrier substrates has been pursued to develop compliant substrates that in turn would allow epitaxial growth of widely lattice-mismatched materials. For example, highly strained InGaAs quantum wells could be incorporated between GaAs/AlAs distributed Bragg reflector mirrors to form long wavelength vertical cavity surface emitting lasers (VCSELs). We will discuss our (limited) progress to achieve large area (quarter of 3î wafer) GaAs compliant substrates, and the challenges which remain.

From another perspective, wafer bonding can be used directly accomplish unique device integration. For example, bottom-emitting VCSELs emitting at 850 nm or shorter wavelength are problematic due to absorption in the GaAs substrate. However, this can be problem overcome if the VCSEL epitaxy is wafer bonded to a transparent carrier substrate such as AlGaAs or GaP. We will also discuss the fabrication of large area (quarter of 2î wafer) wafer bonded bottom-emitting VCSELs on transparent GaP substrates.

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Aerodynamic Sensors Using Silicon Nitride Wafer-Bonding Technology

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This paper provides an overview of silicon-nitride/silicon fusion-bonding technology for aerodynamic sensors. The process development and impact on aerodynamic device performance are described. The basic fabrication process combines silicon-nitride/silicon fusion bonding, deep-reactive ion etching and standard lithography to produce dielectrically isolated, single-crystal silicon islands on top of a thin silicon-nitride membrane suspended above a controlled-ambient cavity. Depending on the desired sensor technology, the process can be modified to replace the silicon islands with a variety of thin-film materials. This process yields device structures with strict diaphragm geometry tolerances, device alignment, and thermal isolation. Examples of representative devices fabricated using this technology will be presented. Specifically, the development of a thermal shear-stress sensor and a piezoresistive microphone will be presented.

Study of InGaAs/GaAs Compliant Substrates for Various Applications

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In order to optimize InGaAs on GaAs compliant substrates (CSs), we have varied the wafer bonding temperature, pressure, time, and twist angle. Intensive characterizations including Auger, SIMS, TEM, and Ellipsometry have been performed to verify the quality of CSs. We have grown bulk materials, quantum wells, Mid-IR InAs/InGaSb/InAs/AlSb type-II quantum-well (QW) lasers, Mid-IR type-II photodetectors, and InGaAs/InAlAs Bragg reflectors on the CSs to verify the function of CSs. Impressive results have been achieved in Mid-IR type-II lasers and photodetectors. Additionally, we are optimizing the materials uniformity across 2-inch compliant substrates. Here, we will present some of the preliminary results. The authors of AOI would like to acknowledge the support from Air Force Research Laboratory and National Science Foundation. The authors of AFRL would like to acknowledge the support of Dr. Vaidya Nathan and Dr. David Cardimona of the Air Force Research Laboratory Space Vehicles Directorate (AFRL/VSSS), and Maj. Dan Johnstone of AFOSR.

Alternative Approach to the Growth of HgCdTe IR Detectors

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Infrared detectors based on HgCdTe currently provide state-of-the-art performance for a wide range of detector imaging applications. Growth of HgCdTe by MBE on (211)-oriented substrates of either CdZnTe or Si is used to produce complex detector structures capable of single and multiple-wavelength detection with near-theoretical performance. Focal-plane arrays of HgCdTe detectors are usually fabricated by connecting a detector array chip to a separate Si readout circuit chip through the use of localized indium bump bonding. A future alternative to this technology would be to produce an integrated detector/readout assembly on a single wafer, thus eliminating the need for indium bump bonding. In principle, this can be accomplished by bonding a thin (211) Si layer to a (100) Si substrate, followed by growth of CdTe and HgCdTe epilayers using a growth approach similar to that used for current HgCdTe on Si technology. The challenges of implementing such an approach will be discussed, including the issue of possible compliant substrate behavior in highly lattice-mismatched materials grown at low temperature.

InGaAs Layers Grown by OMVPE on Compliant Substrates for Extended Wavelength Detectors

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Currently extended wavelength InGaAs detectors (>1.7μm) on InP are limited by the lattice-mismatch and consequent introduction of dislocations in the absorbing layer. In order to overcome these limits, GaAs compliant substrates have been introduced for the growth of extended wavelength InGaAs detectors. In a first stage up to 3.8% lattice-mismatched InGaAs growth on GaAs compliant substrates has been investigated. The twist-bonded GaAs compliant substrates have a thickness of typically 30-80 Å and twist angles between 10 and 45° were applied. Wafer bonding was done under pressure in a nitrogen atmosphere at 660°C during one hour. The surface of the compliant substrates was very dependent on the substrate cleaning before bonding (and also overgrowth) and the bonding conditions.

Normarski phase contrast microscopy, room temperature photoluminescence (PL) and double crystal X-ray diffraction (DXRD) were used to characterize the hetero-epitaxial layers. Additional transmission electron microscopy (TEM), high resolution XRD and atomic force microscopy (AFM) was done on some compliant substrates. This resulted in smooth and cross-hatch free surface morphology for InGaAs layers on 60 Å thick GaAs compliant substrates, for a layer thickness exceeding up to 50 times the Matthews-Blakeslee critical thickness. XRD measurements indicate a reduced peakwidth and tilt of the overgrown InGaAs layer, thus indicating a reduced misfit dislocation density.

Consequently highly mismatched (5-6%) and thick (1-2 μm) InGaAs layers for the development of InGaAs detectors up to 2.5 μm, were grown on GaAs compliant substrates. Preliminary results for the dark current of InGaAs detectors developed on compliant substrates indicate a comparable dark current level as for ordinary GaAs substrates, but a significant improvement in dark current uniformity (see Fig.1).

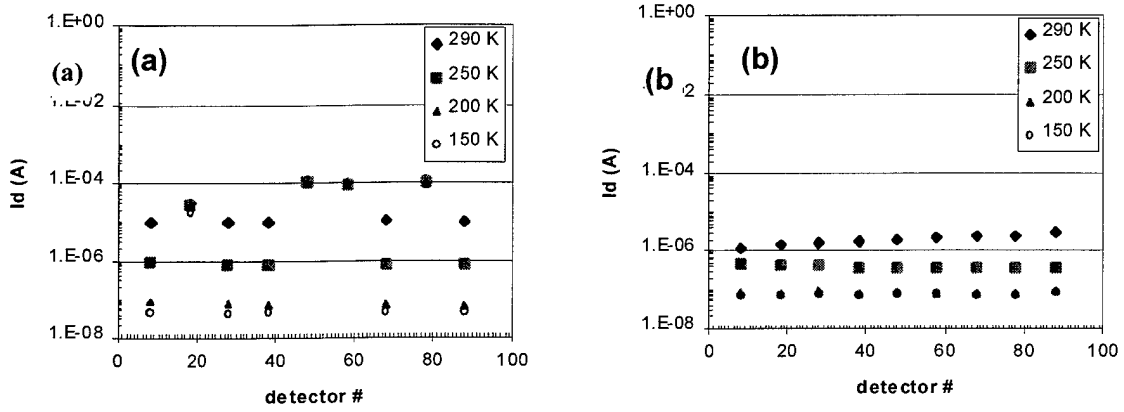

Fig. 1: Dark current measurements (I_d) versus temperature for an $In_{0.70}GaAs$ detector array grown on (a) an ordinary GaAs and (b) a compliant GaAs substrate.

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Strained-layer InAs/InGaSb Superlattices on Compliant GaAs Substrates for Very Long Wavelength Infrared Detection

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A limiting factor in the development of infrared imaging arrays utilizing type-II InAs/InGaSb superlattices is the GaSb substrates used for lattice-matched epitaxial growth. These substrates are conductive, limited to two inch diameters, and are highly absorbing at infrared wavelengths greater than 5 micrometers. This non-transparency in the infrared is incompatible with the standard approach of indium bump bonding arrays to readout circuits and using backside illumination for infrared imaging. An alternative to the GaSb substrates is the use of GaAs substrates with a bonded, thin compliant layer to reduce misfit dislocation formation associated with the large lattice mismatch between GaAs and the superlattice. Type-II superlattices of several different designs have been grown by molecular beam epitaxy on compliant GaAs, as well as GaSb, substrates. The effects of these substrates on the optical, electrical, and structural properties of the superlattice were studied. The superlattices grown on the compliant substrates were found to have low dislocation densities, uniform layers, excellent electrical isolation from the substrate, and improved infrared photoresponse. The development of superlattices on compliant substrates is a more cost effective approach to addressing the GaSb substrate limitations for infrared imaging than a program to improve the bulk crystal growth of GaSb.

Compliant and Alternative Substrate Requirements for Low Cost, Light Weight, High Efficiency Solar Cells

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Several universities, government laboratories, and companies are investigating compliant and alternative substrate technologies for various electronic and optoelectronic applications, including space solar cells. Space solar cells are an immediate market opportunity for compliant substrates because of the large volume of wafers used to meet the present and growing space satellite power needs. Also, the primary tangible benefits of compliant substrates, i.e., lower cost and lighter weight, have great market potential because of the high cost of launching satellites and of the high efficiency solar cells themselves.

However, space solar cells have unique and very stringent requirements that must be met prior to implementation. In fact, the present growth and processing techniques that are used to fabricate today's high efficiency solar cells (as high as 27.0%) place very demanding conditions upon the compliant or alternative. On orbit, the solar cells and compliant substrates are subject to acoustic and thermal cycle conditions that can be very severe.

Also, the high efficiency space solar cell market has been driven by the need for high and higher efficiencies, such that any decrease in performance of the solar cells using compliant substrates will limit their application. It has been shown that at the satellite systems level, the higher cost of the higher efficiency solar cells prove to be overall more economical because of reduces weight and launch cost. Also, the high efficiency cells are sometimes mission enabling. Therefore, while the space solar cell market seems to be an ideal application of compliant and alternative substrates, several hurdles must be overcome to meet these requirements prior to application. This paper will review the requirements on compliant and alternative substrates from a space solar cell perspective.

Lateral and Pendeo-epitaxial Growth of GaN and Related Compounds and Alloys on 6H-SiC(0001) and Si(111) Substrates

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Conventional heteroepitaxial growth of GaN on low temperature GaN or AlN buffer layers previously deposited on Al2O3 and SiC substrates results in films containing a high dislocation density (108-1010 cm-2) due to the lattice mismatches between the buffer layer and the film and/or the buffer layer and the substrate. The objective of this research has been the significant reduction in dislocation density in GaN thin films via special methods of MOVPE growth.

Lateral epitaxial overgrowth (LEO) of GaN stripes patterned in an SiO2 mask deposited on GaN film/AlN buffer layer/6H-SiC(0001) substrates was the initial method. The mask contained 3mm and 5mm wide stripe openings, spaced parallel at 3-40mm, and oriented along < > and < > in the GaN film. The deposited material grew vertically to the top of the mask and then both laterally over the mask and vertically until coalescence. The average RMS roughness of the LEO layers was 0.25 nm. This is similar to the values of the seed GaN films. Threading dislocations, originating from the GaN/AlN buffer layer interface, propagated to the top surface of the regrown GaN layer within the window regions of the mask. By contrast, there were no observable threading dislocations in the overgrown portions of the layer. The few dislocations observed formed parallel to (0001) plane via the extension of the vertical threading dislocations after a 90š bend in the regrown region. They did not subsequently propagate to the surface of the overgrown GaN layers.

Recently we have pioneered a new process route to selective epitaxy of GaN and AlxGa1-xN layers with a low-defect density, namely, pendeo (from the Latin: to hang or be suspended from)-epitaxy (PE). It incorporates mechanisms of growth exploited by conventional lateral growth processes by using masks to prevent vertical propagation of threading defects, and extends the phenomenon to employ the substrate itself as a pseudo-mask. The growth does not initiate through open windows, rather it begins on sidewalls of forms etched into a seed layer and continues until coalescence over and between the seed structures occurs, resulting in a single complete layer. The PE growth of GaN and AlGaN alloys via MOVPE and the use of silicon nitride and nickel etch masks has been the focus of this investigation. The three main stages of PE growth, namely (i) initiation of selective lateral homoepitaxy from the seed sidewalls of the nitrides, (ii) vertical growth and (iii) lateral growth over the silicon nitride masked seed structure to form both discrete microstructures and coalesced single crystal layers will be described for these materials. These processing procedures and the aforementioned stages will be presented in tandem with supporting structural, microstructural, optical and electrical evidence.

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GaN on Silicon-on-Insulator (SOI) Substrates And Compliant Growth of Widebandgap Materials

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GaN was grown by low-pressure metalorganic chemical vapor deposition (LP-MOCVD) on compliant Silicon-On-Insulator (SOI) substrates and improved material quality is demonstrated. Crystal quality, surface morphology and electron mobility could be improved by increasing the buffer growth rate. It is shown experimentally that the quality of the grown GaN epilayer can be drastically improved by reducing the thickness of the top Si layer of the SOI substrate, as theoretically expected for growth on compliant substrates.

Photoluminescence (PL) measurements show that the peak position of the UV emission changes both with measurement temperature and strain. At room temperature, the UV peak is red-shifted by 64meV corresponding well to the bandgap temperature dependence. Strain-induced blue shift of the peak, compared to unstrained GaN, is much less than for growth on sapphire, indicating strain-relief in the GaN by growth on SOI. Further reduction of the blue shift is consistent with increased electron mobility.

Details of GaN growth and obtained material parameters will be presented and the impact of compliant growth technology on the quality of widebandgap materials will be discussed.

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Compliant Substrates for GaN and Strain Modulated Epitaxy

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Alternative substrates for GaN growth such as lithium gallate (LGO) are promising due to their close lattice match and relative ease of removal. We are investigating the growth of GaN on LGO to enable thin film GaN substrates for regrowth and for applying packaging techniques for improved heat removal for devices. We will discuss new structural data related to the GaN/LGO interface and improved heterostructure properties. In addition, we are investigating the use of deposited metal layers for engineering bonds that reduce thermal strain during the growth of materials with different CTE mismatches. We are applying this approach to GaN and GaAs materials and will discuss current results.

Lateral Epitaxial Overgrowth Using Alternative Sources

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The use of diethyl gallium chloride (DEGaCl) was studied as an alternative gallium source and compared to the use of trimethyl gallium (TMGa) for the Lateral Epitaxial Overgrowth (LEO) of GaN by Metal Organic Vapor Phase Epitaxy (MOVPE). The decomposition of DEGaCl to GaCl produces growth conditions similar to those found in the Hydride Vapor Phase Epitaxy (HVPE) technique near the growth front producing increased lateral growth rates. The highest lateral-to-vertical growth ratio achieved was ~5 for the DEGaCl-based growth as opposed to ~4 for TMGa-based growth at high growth temperature and high V/III ratio for openings aligned along the $<1\bar{1}00>$ direction. Controlled vertical and sloped facets were produced through the choice of the reactor operating conditions. LEO GaN using DEGaCl source has smaller kink density along the growing facets, which is desirable for fast and smooth coalescence under conditions, required for improved material properties. The surface morphology and the structural and optical properties of the coalesced LEO GaN revealed improved GaN materials in the ELO region with a significant reduction in dislocation density as characterized through AFM, TEM and low temperature PL. The difference in LEO behavior for the two Ga sources is discussed in terms of the chloride-based growth chemistry and existing models of HVPE growth.

Nanostructured SOI Compliant Substrates

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Substrate nanostructuring invokes geometrical and materials properties effects that have a potential for creating new epitaxial process routes. The theory of nanoheteroepitaxy (NHE) has shown that three-dimensional geometrical effects can be implemented to enhance the strain partitioning and lower the strain energy in heteroepitaxial layers grown on nanostructured compliant substrates. NHE theory predicts that the strain energy is lowered because the strain in nanoscale islands partitions into the substrate and epitaxial materials and decays exponentially away from the interface with characteristic length of decay proportional to the diameter of the island. In materials systems which possess a lattice mismatch in the range of 0-4%, the NHE predicts that the strain energy is lower than that required to nucleate a screw dislocation provided that the island diameter is sufficiently small.

In addition, the ability to control materials properties by changing size and dimension will also enable atomically engineered materials with tailored properties to assist in the epitaxy of lattice mismatched materials systems. For example, a size induced lowering of the melting temperature of silicon nanomesas has been observed. The reduced melting point is near the growth temperature of GaN, ~1050 °C. Due to growth near the melting temperature of the silicon nanomesas, it is expected that the Young's modulus of the silicon nanomesas is also reduced during growth, having the effect of enhancing strain partitioning and substrate compliance. This paper will describe geometrical and materials properties effects of nanostructuring <111>SOI. The transmission electron microscopic and photoluminescence characterization of GaN grown on nanostructured and planar <111>SOI, and planar Si(111) substrates will be presented.

Systematic Study of SIMOX SOI Structures as Compliant Substrates for SiC and GaN[1]

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In this work, we are investigating use of silicon-on-insulator (SOI) structures produced using the SIMOX process as compliant substrates for epitaxial growth of large area SiC and GaN films. High crystalline quality cubic SiC layers of up to 40 microns thick have been grown on 2- and 3-inch diameter Si and SIMOX SOI substrates using a two-step growth process. The first step involves conversion of surface silicon layer of a SIMOX SOI wafer through high temperature carbonization, followed by epitaxial SiC growth step using atmospheric chemical vapor deposition (CVD). Results from systematic study of crystalline quality by means of X-ray diffraction (XRD) and transmission electron microscopy (TEM) for the resultant SiC-on-SOI structures will be discussed.

We are also investigating the feasibility of using SiC-on-SOI structures as compliant substrates for growth of GaN layers. The latest data on crystalline quality of GaN/SiC/SOI structures as measured by TEM and electron diffraction, as well as photoluminescence study will also be discussed.

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Compliant Substrates for Silicon Carbide Growth

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Devices made from silicon carbide (SiC) have the potential to fulfill many of the required properties of next generation high performance electronics. Presently, commercial SiC substrates are available in the 6H and 4H polytypes. Substrate defects (including micropipes and etch pits) and high substrate cost continue to be barriers to commercialization of SiC devices.

High quality SiC alternatively can be grown by epitaxial growth. Unfortunately, present growth processes result in epilayers containing mixed phase polytypes and high background dopant levels. An innovative silicon carbide growth process based on pulsed seeded supersonic beam deposition has been developed. The increased kinetic energy available with a seeded supersonic beam enables homoepitaxial SiC films to be deposited at lower growth temperatures, which improves quality and potentially reduces the cost of device fabrication.

An enabling technology for development of reliable, cost effective SiC devices is then a low cost substrate technology for deposition of SiC epilayers. The lower temperature deposition afforded by the supersonic beam deposition technique is directly compatible with the low melting temperature of silicon (1420°C). 3C SiC, which grows on Si, has many of the electrical properties desired for SiC semiconductor devices. When SiC is grown on silicon (Si), only localized domain growth is observed due to the large SiC-Si lattice mismatch. Compliant silicon (Si) substrates, designed to overcome the SiC-Si lattice mismatch, may alllow domain-free growth of 3C SiC.

Development and performance of a multiple jet reactor capable of depositing doped, epitaxial SiC films up to 2" diameter will be described. Deposition rates, film quality, and doping levels will be discussed, as well as a comparison of the supersonic seeded beam deposition method with conventional epitaxial growth processes. 3C SiC heteroepitaxy on Si and Si twist-boundary compliant substrates will be discussed.

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Recent Advances in High-Brightness Transparent-Substrate AlGaInP Light-Emitting Diodes: The Road Towards Viable Solid-State Lighting Sources

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Recently, very rapid and substantial progress in the performance and cost of transparent-substrate AlGaInP light-emitting diodes has occurred. Specifically, the development of multi-well active layer structures which combine high internal quantum efficiency and minimal self-absorption have resulted in significant improvements in both the internal and light-extraction efficiency of these devices. These advances, combined with shaping of the chip geometry to form high-power truncated inverted pyramid (TIP) LEDs, have resulted in devices which exhibit a luminous efficiency >100 lm/W with a peak light-output of 60 lm (610 nm peak wavelength) and 55% external quantum efficiency with a peak output power >400mW (650 nm) under DC room-temperature operation (300 K). Furthermore, scaling the geometry of the metalorganic chemical vapor deposition (MOCVD) growth and compound semiconductor wafer bonding processes to 75-mm diameter wafers with simultaneous improvements in process yields and increases in production volumes have driven substantial decreases in the cost of these devices. The result of these advances is an improvement in both the efficiency and flux per emitter as well as a decrease in the cost per lumen for high-brightness LEDs in a fashion that parrallels Moore's Law in the electronics industry.

Compliant Substrates: A Comparative Study of the Relaxation Mechanisms of Strained Films Bonded to High and Low Viscosity Oxides

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The relaxation mechanisms of heteroepitaxial films grown on compliant substrates is presently being studied by many groups. Several compliant substrate concepts have been proposed for the growth of low dislocation, relaxed heteroepitaxial films including silicon-on-insulator (SOI) substrates[i], twist-bonded substrates[ii], and free standing films[iii]. In this work the relaxation of pseudomorphic strained SiGe films transferred by wafer bonding to high and low viscosity oxides is studied. This can best be described as a ìstrain-relaxedî compliant substrate and effectively decouples the growth mechanisms from compliant substrate tenets. Upon thermal annealing, film relaxation is observed with both oxides studied but the behavior is dramatically different. Low viscosity oxides allow film relaxation to occur by viscous flow at temperatures *above* the glass transition temperature, T_g. In contrast, relaxation on high viscosity oxides occurs at temperatures *below* T_g. The absence of film relaxation below T_g for the low viscosity oxide indicates that plastic flow at the film/oxide interface must be responsible for relaxation on high viscosity oxides. A detailed comparison between the relaxation behavior on high and low viscosity oxides is made using atomic force microscopy (AFM), transmission electron microscopy (TEM) and x-ray diffraction (XRD).

The strain-relaxed compliant substrates were fabricated by novel film transfer technique[iv] that combines the SOI fabrication techniques of separation by hydrogen implantation (Smart-Cut[v]) and bond-and-etch-back[vi]. Using this technique fully strained epitaxial 30 nm $Si_{0.7}Ge_{0.3}$ films were transferred to 100 mm oxide coated Si handle wafers. Two oxides were investigated: 120 nm dry thermal SiO_2 ($T_g \approx 1150\_C$[vii]) grown at 1000_C; and 200 nm of borophosphosilicate glass (BPSG: 4.4 w/o B and 4.1 w/o P; $T_g \approx 675$[vii]) deposited by CVD and annealed at 900_C. A thin intermediate layer of epitaxial Si (4 nm) between the SiGe and oxide layers provided reproducible hydrophilic bonding conditions. The as-fabricated films were characterized by AFM, TEM, and XRD which indicated that the films were very smooth (RMS roughness≈0.1 nm), fully strained and dislocation free.

Film relaxation was investigated through thermal annealing studies all of which were carried out in a furnace typically for 90 min in N_2 ambient. In the case of the thermal SiO_2 no change in strain was observed until the highest temperature studied, 975_C. At this point the film relaxed approximately 60%. The RMS surface roughness was unchanged. Cross sectional and plan view TEM revealed that a moderate density (~10^4 cm^{-1}) of stacking faults or microtwins had nucleated throughout the film. Careful examination of the micrographs, however, revealed no misfit dislocations in the partially relaxed film in contrast to observations in previous studies[i].

Significantly different behavior was observed in the case film relaxation on BPSG films. AFM characterization showed a strong increase in RMS surface roughness above the BPSG glass transition temperature. XRD however revealed no significant relaxation up to 800_C at which point the signal from the 004 SiGe reflection was extinguished. The SiGe film was found by SEM to be continuous and composed of periodic undulations with a period of ~1 μm and an amplitude of 70-80 nm. A one dimensional sinusoidal least squares fit to these undulations revealed that the linear surface distance perpendicular to the undulations had effectively increased by 1.05%. This is consistent with the requirement that the 1.2% compressively strained film *expand* laterally by that amount in order to fully relax. To verify that film expansion resulting from strain relaxation produced the undulations, an as-fabricated, unannealed portion of the wafer was patterned into an array 30x30 μm^2 mesas by standard photolithography and plasma etching techniques. The patterned sample was annealed as before at 800_C. XRD showed that the SiGe mesas had relaxed approximately 85% and AFM revealed that the surface roughness was ~0.1 nm.

The comparison of relaxation behavior on high and low viscosity oxides indicates that in the former case relaxation must occur through plastic flow at the interface between the film and oxide as first pointed out by Powell et al[i]. This type of plastic flow, however, is not observed on the low viscosity BPSG oxides and the conclusion then is that temperatures in excess of 900_C are required for Si/SiO_2 plastic flow.
This first demonstration of a strain-relaxed compliant substrate utilizing a low viscosity oxide illustrates that film relaxation can occur elastically if lateral film expansion is allowed. In fact, film expansion or contraction must be accounted for and it remains to be seen if elastic film relaxation over large areas is possible with any compliant substrate technology.

References:
[1] c.f. A.R. Powell et al., Appl. Phys. Lett. 64, 1856 (1994); Z. Yang et al., J. Vac. Sci. Technol. B 16, 1489 (1998).
[1] F.E. Ejeckam et al., Appl. Phys. Lett. 71, 776 (1997).
[1] c.f. F.E. Ejeckam et al.., Appl. Phys. Lett 70, 1685 (1997); A.M. Jones et al., Appl. Phys. Lett. 74, 1000 (1999).
[1] K.D. Hobart et al., Elec. Lett. 34, 1265 (1998).
[1] M. Bruel, Elec. Lett. 31, 1201 (1995).
[1] D. Godbey et al., Appl. Phys. Lett. 56, 373 (1990).
[1] K. Nassau et al., J. Electrochem. Soc. 132, 409 (1985).

Compliant Substrate for High Power Optically Pumped Mid-IR Lasers Applications

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High-power mid-infrared (MIR) lasers are highly desirable for a variety of applications such as remote chemical sensing, infrared countermeasures, environmental monitoring, etc. We will report the recent progress in the development of optically pumped Mid-IR lasers based on InAs/InGaSb/InAs/AlSb type-II quantum wells (QWs) on GaAs compliant substrate for high power applications. Previously, devices reported by our group and others have had fairly good performance in low temperature and short duty-cycle operating modes, but have had difficulty at higher temperatures, particularly at large duty cycles. This has been found to be due to a strong rise in internal loss as the temperature is increased. This rising internal loss is responsible for low quantum efficiency at higher temperatures. In order to decrease overall internal loss and improve the high temperature operation of optically pumped laser, the work described herein uses epi-side-down mounting to reduce active region temperature. We will report data from the first wafer of this type, grown by MBE , which demonstrates a peak power of ~250 mW per facet with a 500 μs pulse and 25% duty cycle.

Strain Relaxation in $In_xGa_{1-x}As$ Lattice Engineered Substrates

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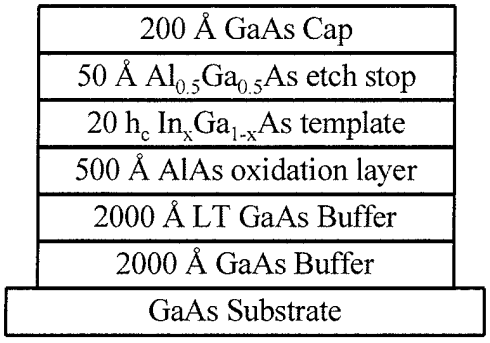
We demonstrate an approach to fabricate quasi-substrates of arbitrary lattice constants. This utilizes the process of relaxation of a coherent hypercritical thickness ($h > h_{critical}$) strained semiconductor over-layer ($In_xGa_{1-x}As$) in direct contact with an oxidizing Al-containing semiconductor (i.e. AlAs or AlGaAs). The process of strain relaxation is studied by varying the strain in the as-grown $In_xGa_{1-x}As$ template and by varying the nature of the $In_xGa_{1-x}As$/oxide interface. Changing the Indium composition in the template varies the strain in the template and the initial misfit dislocation density. Varying the oxidation temperature controls the nature of the $In_xGa_{1-x}As$/oxide interface. The epitaxial structures investigated in this study consisted of strained $In_xGa_{1-x}As$ template layers grown on AlAs oxidation layer on a GaAs substrate. The indium compositions investigated were 20 %, 30 % and 40 %. The thickness of the $In_xGa_{1-x}As$ template layers was 20 times the Matthews-Blakslee critical thickness for each composition. The $In_xGa_{1-x}As$ template layers were grown by molecular beam epitaxy at low temperature (400-430 °C) to minimize the formation of threading dislocations and maintain a two-dimensional growth front. The as grown InGaAs templates show a smooth surface morphology with a rms roughness less than 10 Å and low threading dislocation density as evidenced from Cross sectional TEM micrographs. After growth the substrate was patterned using photolithography and reactive ion etching into 100 µm x 100 µm square mesas to enable lateral oxidation of the AlAs layers. The degree of strain relaxation was determined by X-Ray diffraction of as-grown and oxidized templates. Off-axis (115 and -1-15) X-ray diffraction scans were used to determine the in-plane and out-of-plane lattice constants. Self-consistency of the measurements was checked by on-axis (004) X-ray diffraction which was used to determine out-of-plane lattice constant independently.

The strain is $In_xGa_{1-x}As$ templates was reduced after oxidation as observed from increased strain relaxation. X-Ray diffraction measurements of thermally annealed InGaAs templates under the same conditions revealed no strain relaxation. This indicates is that enhanced strain relaxation is not due to increased thermal energy but is caused by the process of oxidation at the InGaAs/AlAs interface. The degree of strain relaxation in $In_xGa_{1-x}As$ templates was found to increase with oxidation temperature, whereas the efficiency of strain relaxation of found to decrease with the Indium composition. For an $In_{0.2}Ga_{0.8}As$ template the strain relaxation can be increased from 35% for an as-grown template to 90% for a template oxidized at 450 °C. However in the case of an $In_{0.4}Ga_{0.6}As$ template the degree of strain relaxation changes from 57% for an as-grown template to 70% for a template oxidized at 450 °C. It is proposed that the enhanced strain relaxation is due to enhanced movement of threading dislocation due to stresses generated during the lateral oxidation process. Also the porous $In_xGa_{1-x}As/Al_2O_3$ interface minimizes the interaction of threading dislocations with existing misfit dislocation segments, a mechanism which limits strain relaxation in conventional approaches like direct growth. The reactive removal of misfit dislocation cores during the process of oxidation further reduces barriers to threading dislocation motion. Increased oxidation temperatures result in a more porous interface and enhanced removal of misfit dislocation cores and therefore increase the degree of strain relaxation. On the other hand, the misfit dislocation density increases with Indium composition and reduces the efficiency of strain relaxation by increasing the barriers to threading dislocation motion. The relaxed InGaAs layers can be used as quasi-substrates **(Lattice Engineered Substrates)** for growth of material systems with lattice constants between the commercially available binary III-V substrates. Additional results related to growth of long wavelength optoelectronic materials on these substrates will be presented at the workshop.



In (%)	Thickness	T_{growth}
20 %	1300 Å	430 °C
30 %	760 Å	430 °C
40 %	480 Å	400 °C

Figure 1: Layer structure of $In_xGa_{1-x}As$ Templates for Lattice Engineered Substrates

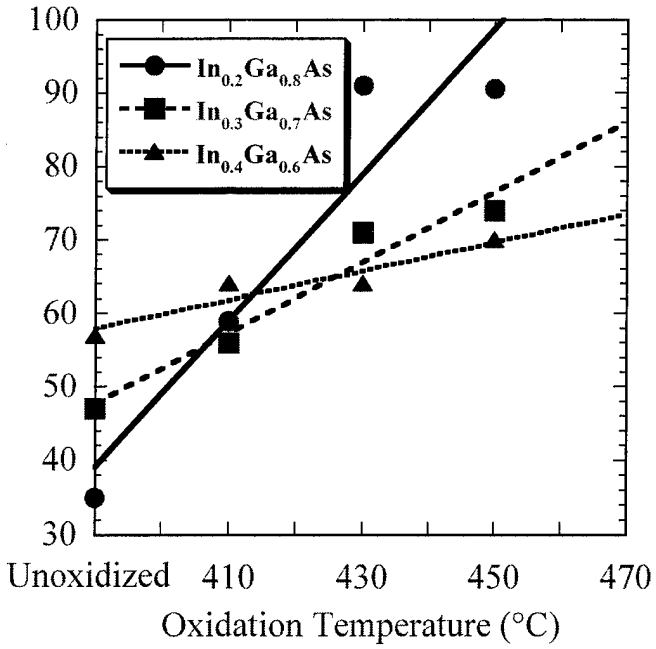
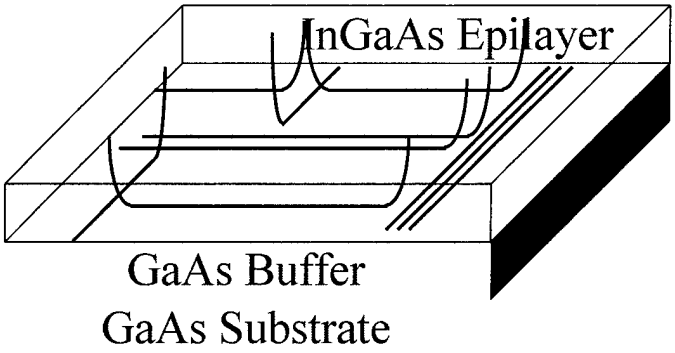
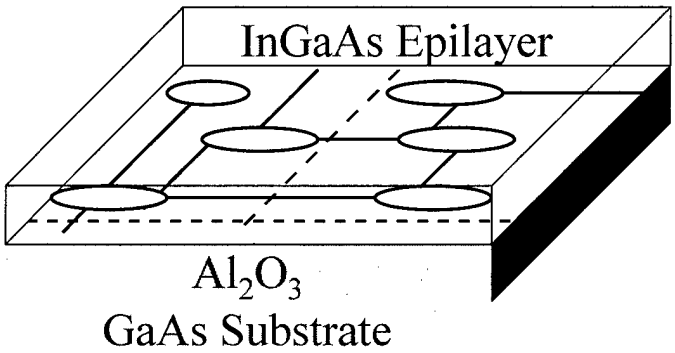


Figure 2:Variation of Strain relaxation for different $In_xGa_{1-x}As$ templates as a function of AlAs oxidation temperature



Conventional Heteroepitaxy
Rigid InGaAs /GaAs Interface
Misfit dislocation interaction :
- Dislocation blocking creates slip bands and pile-ups
- Dislocations bend into the epilayer
- Prevents strain relaxation



Lattice Engineered Substrates
Porous InGaAs /Al_2O_3 Interface
- No dislocation bending and pile ups as there is no dislocation blocking
- Enables strain relaxation
- Reactive removal of dislocation cores and associated strain fields due to void formation

Fig. 3: Strain relaxation mechanism in Lattice Engineered Substrates

SiGe FET Structures on Silicon-on-Sapphire Substrates*

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Silicon-on-insulator (SOI) substrates are of interest for CMOS applications and silicon-on-sapphire (SOS) substrates offer some advantages compared to SIMOX or bonded SOI substrates that have only a thin buried oxide layer. We have fabricated MOSFETS with and without a strained SiGe channel on SOS substrates and shown that the device performance is enhanced by the strained SiGe channel [1,2]. More recently we have fabricated p-channel modulation-doped FET (p-MODFET) devices on bulk Si substrates [3,4] and on SOS substrates [5]. The p-MODFETs have significantly enhanced performance compared to the SiGe MOSFETs.

However, the relatively high densities of defects in the Si layer deposited on sapphire, even after the Si layer is substantially improved by an amorphization and solid phase regrowth process [6], limit the applications of these substrates, especially for SiGe FETs. The effects of the defects on the growth of SiGe device structures by UHV/CVD [7] will be presented.

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1. S.J. Matthew, W.E. Ansley, W.B. Dubbelday, J.D. Cressler, J.A. Ott, J.O. Chu, K.L. Kavanagh, P.M. Mooney, B.S. Meyerson and I. Lagnado, Technical Digest 1997 Device Research Conference, pp130-131, 1997.
2. S.J. Mathew, G. Niu, W.B. Dubbelday, J.D. Cressler, J.A. Ott, J.O. Chu, P.M. Mooney, K.L. Kavanagh, B.S. Meyerson and I. Lagnado, Electron Device Letters **20**, 173 (1999).
3. R. Hammond, S.J. Koester and J.O. Chu, Electronics Lett. (in press).
4. R. Hammond, S.J. Koester and J.O. Chu, submitted to Electron Device Letters.
5. R. Hammond, S.J. Koester and J.O. Chu, J.A. Ott and P.M. Mooney, unpublished.
6. S.S. Lau, S. Matteson, J.W. Mayer, P. Revesz, J. Gyulai, J. Roth, T.W. Sigmon and T. Cass, Appl. Phys. Lett. **34**, 181 (1979).
7. B. S. Meyerson, Appl. Phys. Lett. **48**, 797 (1986).

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